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# Implementation of 13T SRAM Using Power Gated Techniques

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**ABSTRACT**: Static Random Access Memory (SRAM) has become a key factor in new modern VLSI systems. In this paper presents, a design ofSchmitt Trigger based 13Transistor SRAM cell is to be proposed. To minimize the power in 13T SRAM cell using Power gating and Clock gating techniques. This Proposed cell achieves significant improvements in power consumption, Delay and Noise. It can be simulated using 0.25 µm CMOS process technology and also compared their simulation results with 11T SRAM cell. It can operate at a lower supply voltage of 300 mV. Finally 13T SRAM cell are implemented in 4×4 SRAM architecture .These qualities of the proposed design make it for high performance memory chips in the semiconductor industries.

**KEYWORDS:** SRAM, CMOS integrated circuit, Power gating, Clock gating, 4×4 SRAM array

## I. INTRODUCTION

Memory is an essential part of computer and memory chip based systems. All recent systems have been possible by the development of inexpensive and consistent VLSI semiconductor memory chips utilizing NMOS and CMOS technologies. A static Random Access Memory (SRAM) is one in which any location can be accessed in a random manner and thus has equal access time for all memory locations. As well as RAM is volatile chips memory in which both read and write operations performed. Any random memory location can be accessed for information transfer to address, it can read or write from the memory is also called as Read-Write Memory (RWM). Semiconductor memory is divided into two types that are static and dynamic. The static RAM employs bipolar or MOS flip-flops and the dynamic RAM use MOSFETs and capacitors that store data. SRAM, being a key component of the processing system of sensor nodes, has to satisfy the low-power requirement as well. As feature size shrinks the key component of power consumption will be leakage. Leakage power is reduced using different methods that are voltage scaling, transistor scaling and the use of sleep transistors. The 6T SRAM cell is to maintain the circuit performance and energy efficiency but it has to increase the complexity [6].The new 9T SRAM cell has to improve read write stability and to reduce the operating operating voltage but in SRAM area complexity also high. JayhkdeeP.Kulkarni, K. Roy [7]The proposed ST based 10T bit cells had a built-in feedback mechanism to achieving process variation tolerance -a must for nano-scaled technology nodes for low voltage and power consumption ,but speed& system architecture very complex in this design.A. Islam and M. Hasan [8] the cell achieves low power dissipation due to its series-connected tail transistor and read buffers, which offer a stacking effect, will increase a delay in designs.

## II. EXISTING 11T SRAM CELL

TheST11T SRAM cell consists of a cell core (cross-coupled ST inverter), a read path consisting of two transistors, and a write-access transistor. The write-access transistor Q11 is controlled by row-based WL, and the read-access transistor

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Q8 is controlled by row-based read WL (RWL). The feedback transistors nearby Q5, Q6 are controlled by internal storage nodes Q and QB, respectively, with their drains connected with a control signal Wordline_bar (WLB) (inverted versionof write enable signal).WLB and BLs (BL and RBL) are column-based.[1]

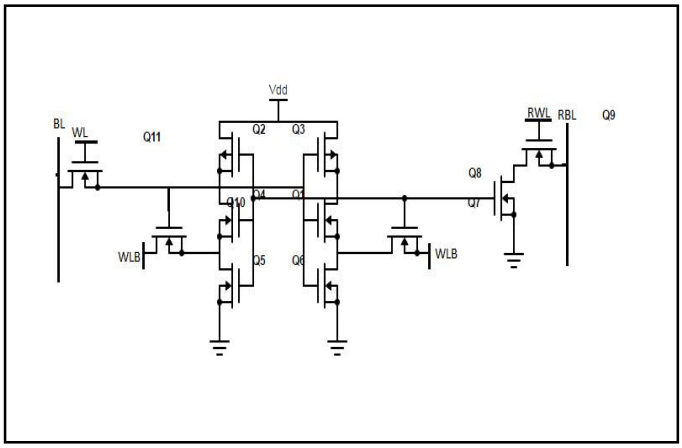


Fig.1. Existing 11T SRAM Cell

If the memory is floorplanned, such that all the cells of a word are adjacent to every cell.

*Hold mode*

In hold mode, WL and RWL lines are disabled. The transistors are in isolated condition it holds the data in Q node.

*Read mode*

In read operation RWL are enabled which provides discharging path for RBL through transistors Q6 and Q7 Depending on the data stored at QB. The disabled WL makes data storage nodes (Q and QB) decoupled from BL during the read access.

*Write mode*

For writing data into the cell, WL is activated to transferthe data to storage node from BL, which is set/reset accordingto the data to be written. RWL is disabled.

*Sayeed Ahmad, Mohit Kumar Gupta, Naushad Alam, and Mohd Hasan* [1],proposed 11T SRAM cell are designed.It improves the read write stability but increase in delay noise and power. To overcome this problem we have to proposed 13T SRAM design and also reduction of leakage power and dynamic power consumption using power gating and clock gating techniques also designed with new 13T SRAM cell.

## III. PROPOSED 13T SRAM DESIGN

The proposed work is enchanced design and simulation of Schmitt-trigger based 13T configuration to study its behaviour in nano scale technology node using simulation software Tanner EDA Tool. The schematic of the proposed design will be based on modifying the existing SRAM Cellconfigurations. The various parameters for the design of power and performance metric based onpower, delay, noise can beconsidered for developing the proposed SRAM Cell.[2]

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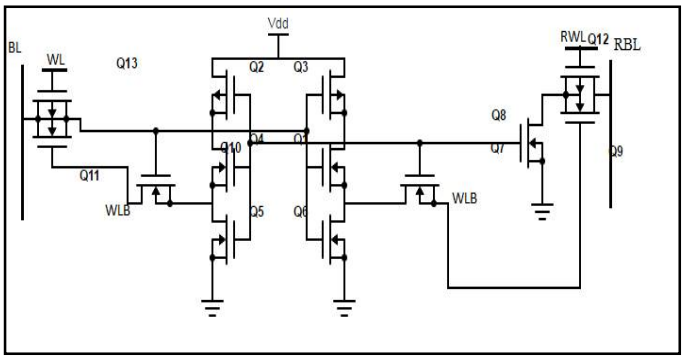


Fig.2. Proposed 13T SRAM Cell

The gate leakage current based power dissipation, delay, noise effect of performance metric will beanalyzed by making use of simulated. The ST based 13T Static-RAM cellconsists of a cell core (cross-coupled STinverter), a read path consists the two transistors, read and a Write-Access (WA) transistor. The architectural change in theproposed schematic is the use of transmissiongates in the access path. The transmission gate passes over the entire voltage range, i.e. strong '0' and strong '1' which improves the optimization of the designed SRAM Cell will also be carried out for low power ,low delaydesign. The write-accesstransistor is controlled by row-based Word Line (WL), and the read-access transistor is controlled by row-based Read Word Line (RWL). The feedback transistors of ST nearby Q5 and Q6, and are controlled by internal storage nodes Q and QB respectively, with their drains connected with a control signal Wordline_bar (WLB) gnd inverted version of write enable signal).BL and RBL are columnbased. Sleep transistorspower gating technique is used whichminimizes the power dissipation. The power gating techniques are used toreduce the power consumption of the circuit.

### *A .PROPOSED 13T SRAM USING POWER GATING*

The Proposed ST13T SRAM cell has different modes of operation. During the hold mode, both Word Line (WL) and Read Word Line (RWL) are disabled and GND is kept grounded [3],[4]. Therefore, the cross-coupled Schmitt Trigger inverter is isolated from both the Bit Lines (BLs), and the data-holding capability is increased due to the feedback mechanism.

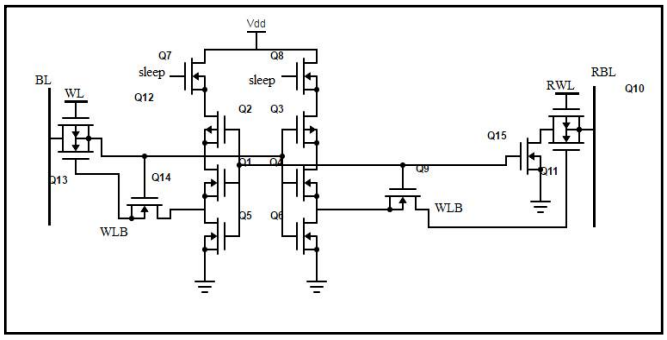


Fig.3. Proposed 13T SRAM using Power Gating

In the read operation, Word Line (WL) isdisabled, whereas Read Word Line (RWL) isenabled, which provides discharging path forRead Bit Line (RBL) through transistors depending on the data stored atQB. The disabled Word Line (WL) makes data storage nodes (Q and QB) decoupled from BL lines.Bit line (BL) during the read access. The storage node may not get disturbed duringRead operation. It is to be noted that in bothread and hold mode, WLB is at *V*dd (becausewrite enable signal is disabled), which helps the feedback transistors nearby Q5 and Q6 toprovide a feedback mechanism and to exploitthe feature of ST inverter to have a goodinverter characteristic.For writing data into the cell, WL is activatedto transfer the data to storage node from BL,which is set/reset according to the data to

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bewritten. RWL is disabled,The WLB signal, which is inverted versionof write enable signal, is disabled (i.e., WLB =0 V) during the write operation. Consequently,there is no feedback action from any of the feedback transistors N5 and Q6[3],[4],[5] as thevoltage at nodes does not rise.Subsequently, the writing speed is significantlyincreased.The data retention phase is when the databit is held in the cross-coupled inverter pair.During this phase the power requirement ofthe circuit is very less therefore, the SLEEPsignal is activated during this phase for theleakage power reduction. This technique is known as the power gating technique. Thereare many possible choices for the power gatingtechniques but in this paper the sleep transistortechnique is used. The sleep transistors are turned ON duringthe active mode, in such a way that the normal operation is not affected as there exist a pathbetween the supply and the ground rails. Thesleep transistors are turned off in standbymode, thereby, shutting down the power supplyto the circuit creating virtual supply and groundrails. This technique is popularly known as sleep transistors.

### *B. PROPOSED 13T SRAM USING CLOCK GATING*

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation.Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flop in them does not have to switch

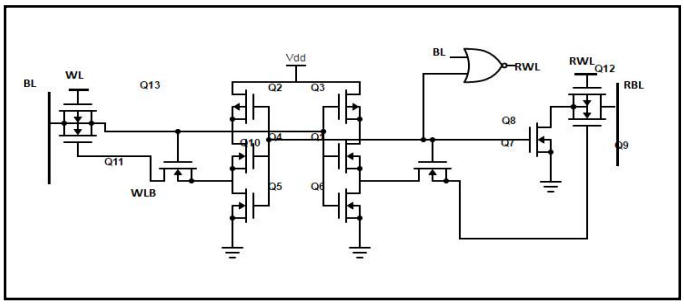


Fig.4. Proposed 13T SRAM using Clock Gating

Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred. Clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks. Therefore it is imperative that a design must contain these enable conditions in order to use and benefit from clock gating. This clock gating process can also save significant die area as well as power, since it removes large numbers of mux's and replaces them with clock gating logic. This clock gating logic is generally in the form of "Integrated clock gating" (ICG) cells. However, note that the clock gating logic will change the clock tree structure, since the clock gating logic will sit in the clock tree. Clock gating logic can be added into a design in a variety of ways: Coded into the RTL code as enable conditions that can be automatically translated into clock gating logic by synthesis tools (fine grain clock gating). Inserted into the design manually by the RTL designers (typically as module level clock gating) by instantiating library specific ICG (Integrated Clock Gating) cells to gate the clocks of specific modules or registers. Semi-automatically inserted into the RTL by automated clock gating tools.[15] These tools either insert ICG cells into the RTL, or add enable conditions into the RTL code. These typically also offer sequential clock gating optimizations. Sequential clock gating is the process of extracting/propagating the enable conditions to the upstream/downstream sequential elements, so that additional registers can be clock gated. Although asynchronous circuits by definition do not have a "clock", the term perfect clock gating is used to illustrate how various clock gating techniques are simply approximations of the data-dependent behavior exhibited by asynchronous circuitry. As the granularity on which you gate the clock of a synchronous circuit approaches zero, the power consumption of that circuit approaches that of an asynchronous circuit: the circuit only generates logic transitions when it is actively computing.

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### *C. IMPLEMENTATION OF 4×4 ARRAY USING 13T SRAM CELL*

### *A. Precharging*

One pre charging circuit is connected for every column to pre charge the complementary bit-lines, BIT and BITN, to precharged "1" state during inactive state of memory as shown in fig. 5. The signal PRECHARGE is used for this purpose. The precharge circuit is isolated from the bit-lines during the memory write and read operation.

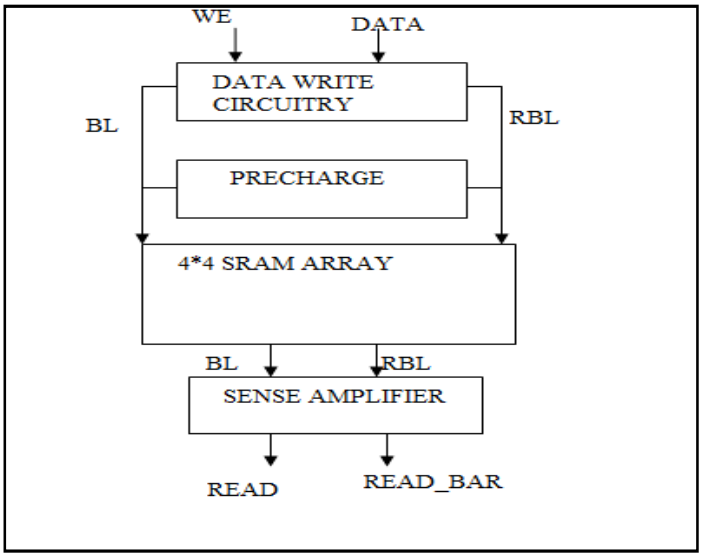


Fig.5. Block diagram for 4*4 SRAM memory system

### *B. Data Write Operation:*

Each of the 4 columns of the memory array has one data write circuit as shown in fig.6. The data write circuit consists of two inverters and an AND gate implemented by pass-transistors. The data write circuitry writes data and its complement onto the bit-lines when activated by write-enable (WE) signal.[14] The data and its complement are written onto the individual nodes Q and QN of the selected word through the access transistors of the SRAM cell[5].

### *C. Data Read Operation:*

The data written into the SRAM cell is retained as long as the power is present. When the memory is idle i.e. when the memory words are not accessed, the feedback provided by the transistors nearby Q5 and Q6 help in retaining the memory status. The gates of transistorsQ5andQ6 are connected to nodes QB and Q respectively as shown in fig. 6. During read operation the sense amplifier enable (SAE) signal is applied to the sense amplifier. This activates the sense amplifier for read operation only for Short sense duration. At the same time the column is isolated from the bit-lines by using signal Ymux. This causes one of the bit-lines BIT/BITN to discharge from the Precharged value.[12] This creates a differential voltage on the bit-lines which is sensed by the sense amplifier and amplified to the full extent. The data and its complement are reflected on the output lines READ;READ_BAR.The fig. 6 shows the top level schematic of 13T SRAM with precharge and sense amplifier.

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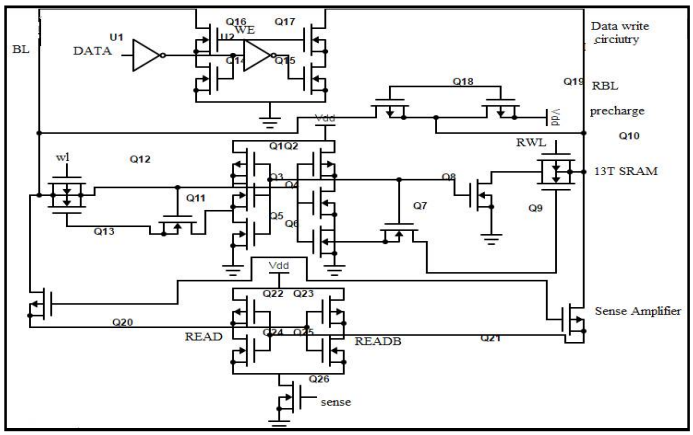


Fig.6. 13T SRAM with precharge and sense amplifier for single bit

The Precharge Circuit is used to precharge the bit-lines, BIT and BITN, to logic „ value during inactive state of memory cell. When memory cell is being written/ read, precharging is deactivated. The *Data Write Circuit* is used to write data and its complement onto the bit-lines. Writing a value into the SRAM cell is done by forcing one of the bit lines (BIT/BITN) high while keeping the other low. To write 1 into the SRAM cell, the word line (WL) is Asserted, bit line BIT is made high and bit line BITN is made low. [11],[12]To write 0 into the SRAM, bit line BIT is made low and BITN is made high. Before reading from the SRAM cell both bit lines (BIT, BITN) are pre-charged high and SRAM cell is selected. When WL selects the SRAM cell to be read, depending on the data in the SRAM cell, one of the bit lines is pulled down. If BIT is pulled down the stored data is 0. If BITN is pulled down the stored data is 1. Sense amplifiersare used to sense which line is being pulled down and perform the read operation of the stored data. READ and READ_BAR indicate the data stored and its complement during the read operation.The single bit memory system comprising of SRAM cell, precharge, data write, column select and sense amplifier is designed and simulated. The complete schematic of data write and read for single cell memory system .This schematic shows all the different peripheral presents[13],[10]s circuits combined with the static RAM cell, to form a complete working SRAM write and read system. The input signals are write enable (WE) that allows writing of data (DATA) to the SRAM cell, sense (SAE) that allows reading of data from the SRAM cell, word line (WL) that decides to/from which address data will be written or read from and the signal data is the one bit data either 1 or 0 that is to be stored into or read from the SRAM cell. The two output signals are READ corresponding to the data signal and READ_BAR is the inverse of data.

## IV. SIMULATIONS AND RESULTS

The simulation results for Power Minimized 13T SRAM using power gating clock gating techniques presented in this section.

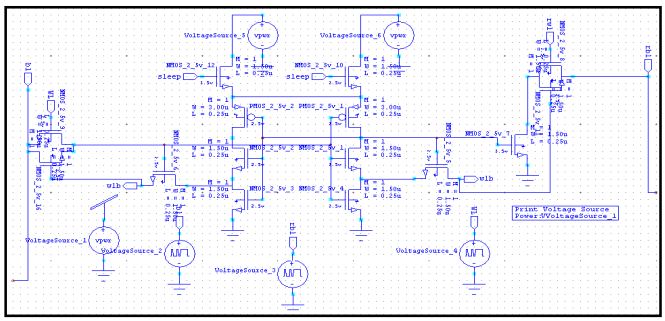

Fig.7. Schematic diagram for 13T SRAM using power gating techniques.

Fig.7. shows that Simulation results for 13T SRAM using Power gating. Here the sleeping transistors are added at header of the circuit for reduction of power in 13T SRAM design.

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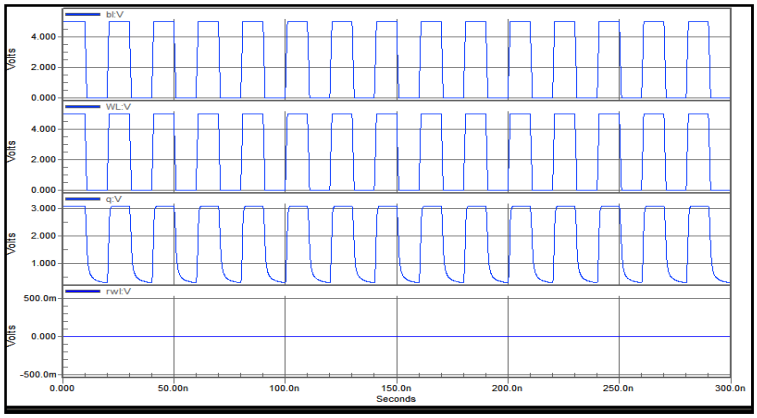


Fig.8. Simulation Result of 13T SRAM Using power Gating for write operation

Fig.8. Shows that simulation result of 13T SRAM using power gating for write operation when BL and WL are enable then q node are charging.

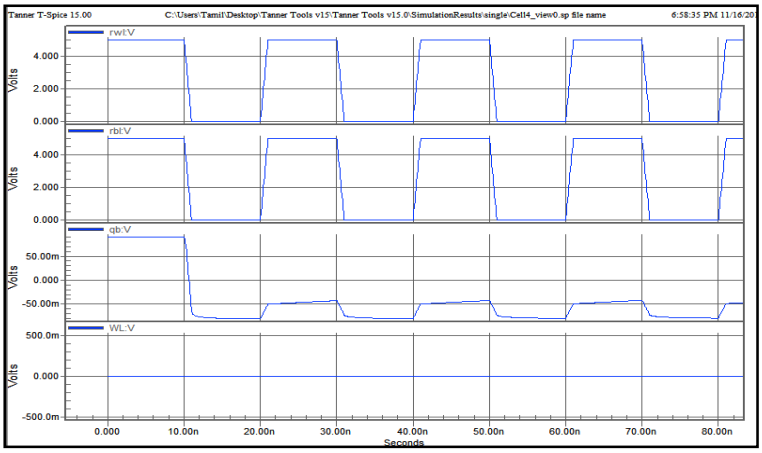


Fig.9.Simulation result of 13T SRAM using power gating for readoperation

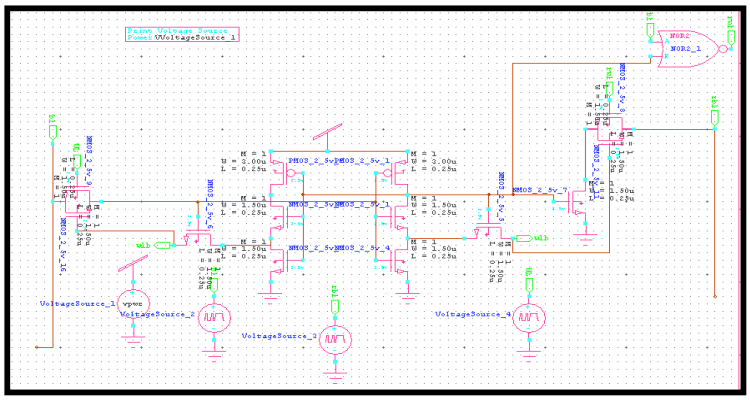

Fig.10. Schematic diagram of 13T SRAM using clock gating

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**Vol. 6, Special Issue 1, March 2017**

Fig.10. shows that Schematic diagram using clock gating which represent the NOR gate are used in 13T SRAM for reducing switching activity.

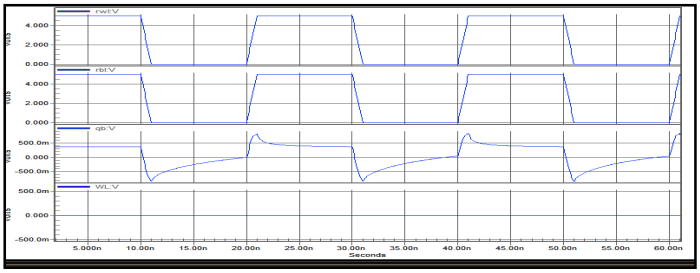


Fig.11. Simulation result for 13T SRAM using Clock Gating for read operation

Fig.11. shows that Simulation result for 13T SRAM using clock gating for write operation.

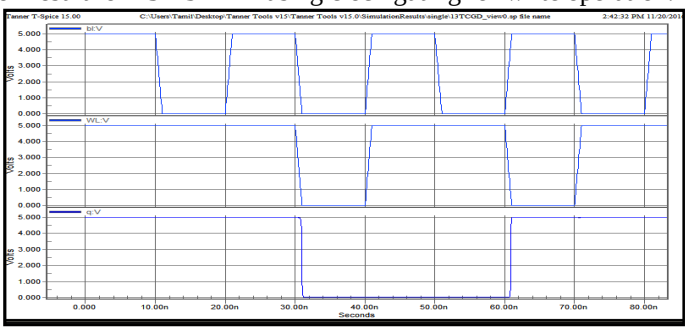


Fig.12. simulation result of 13TSRAM using Clock gating for write operation

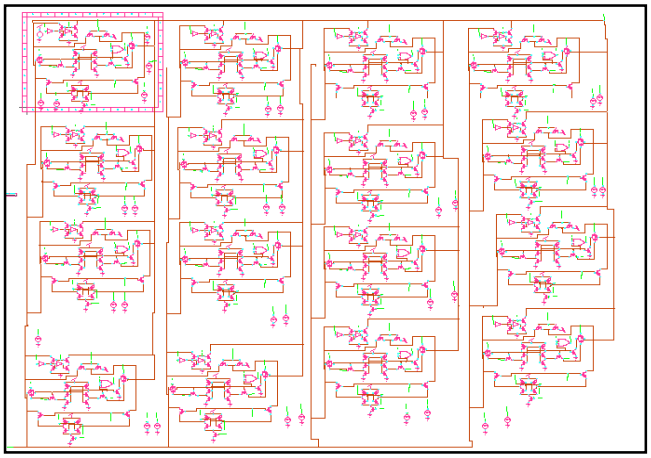

Fig.13. Implementation of 4×4 array using 13T SRAM design

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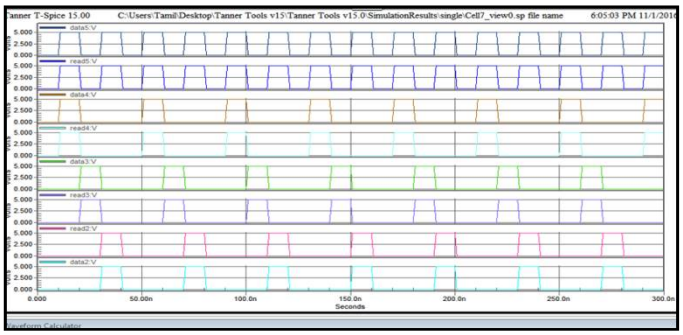

Fig.14. simulation result for Implementation of 4×4 array SRAM

Fig.14. shows that simulation result the data are written in circuit it can be read from sense amplifier through the 13T SRAM.

Tabulation.1.Comparison table for different SRAMbetween Power, Delay, Noise

| Parameter Analysis | 11T SRAM | 13T SRAM | 13T SRAM Using power gating | 13T using SRAM clock gating |
|---|---|---|---|---|
| Power | 1000pw | 284pw | 8.2pw | 4pw |
| Delay | 10000ps | 224.6ps | 137.7ps | 113.6ps |
| Noise | 39.37nv | 19nv | 19nv | 2.6nv |

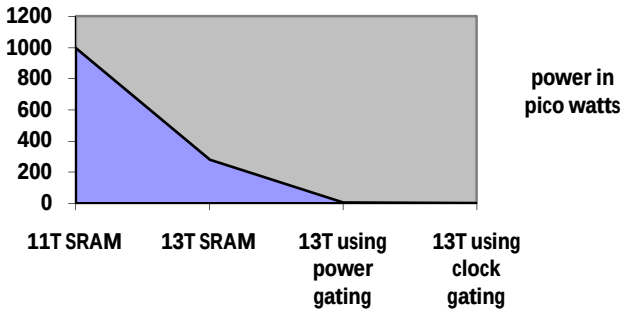


Fig.13.Power Analysis

This figuresshows the trend for the powerdissipation for the designed ST13T SRAM Celland then with the implementation of the powergating technique. As seen from the graph, thepower dissipation is greatly reduced with theuse of the sleep transistors.

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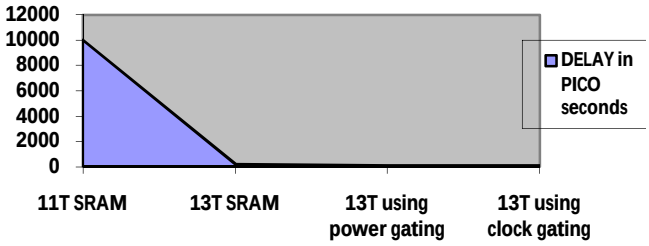


Fig.14. Delay Analysis

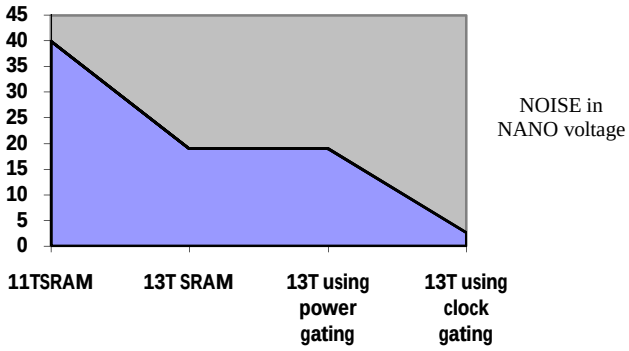


Fig.15. Noise Analysis

This figure15 shows that the Noise analysis for different transistor with clock gating and power gating techniques. For noise voltage mostly reduced in clock gating techniques.

## V. CONCLUSION

The proposed design aims at the power reduction for the Static-RAM cell configurations. From the result it isclear that optimized proposed ST13T Static-RAM Cell is more power efficient with the useof power gating technique, i.e., Sleeptransistors approach. During active mode thesleep transistors are turned ON, so that thenormal operation is not affected as there is apath between the supply and the ground. In this paper also designed 13T SRAM using clock gating approach to reduce the power. Then table shows to minimize the power, delay, noise. Here 13T SRAM using clock gating are high performance circuits compared to other circuit design.This 13T SRAM also implementented 4×4 SRAM array cell with precharge and sense amplifer circuit for read and write operation.

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